DESIGN CONSIDERATIONS IN A BiCMOS DUAL-MODULUS PRESCALER

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ABSTRACT

Design considerations in a dual modulus divide by 32/33 prescaler with a 0.6μm BiCMOS process are presented. Care was taken to design the ECL-based circuits to operate with as low supply voltage and current consumption as possible. The phase noise contribution of the integrated bandgap bias network is demonstrated through simulations. The trade-off between the power consumption and the phase noise is pointed out and some guidelines are provided to improve the noise performance. Measurements confirm the functionality of the prescaler with a 2.5V supply drawing around 2.3mA at 2.35 GHz with an input sensitivity between -24dBm and 12dBm. The circuit operates with a supply voltage down to 2.1V but with limited input sensitivity.

1. INTRODUCTION

Prescalers are among the key building blocks of GHz-range frequency synthesizers used in wireless communication systems, [1], [2]. The quality of the prescaler is vital in setting the performance of the PLL-based frequency synthesizers used as Local Oscillators, especially from the power consumption point of view. There is a continuing research effort to improve the efficiency (i.e. higher operating frequency with lower power consumption) of the prescalers designed with the mainstream CMOS and BiCMOS technologies, [3], [4]. However, the impact of the prescaler phase noise on the PLL output phase noise has not received much attention in the literature. The noise contributors in the prescalers are hardly investigated in the papers causing a lack of understanding to optimize the noise performance of the prescalers designed for wireless communication systems. In this paper, after briefly emphasizing the impact of the prescaler noise on the phase noise performance of the PLL-based frequency synthesizers in Section II, a dual-modulus prescaler design in a BiCMOS technology is presented in Section III. The trade-offs involved in the design are mentioned with emphasis on the phase noise performance. The last two sections include the experimental results and some conclusions, respectively.

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2. PRESCALERS IN PLLs

PLL-based frequency synthesizers are widely used in modern communication systems, mostly in synthesizing well defined, stable local oscillator signals.

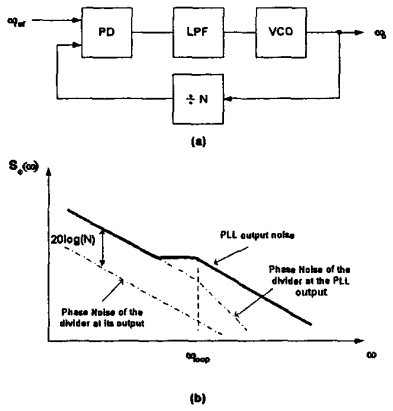

Fig. 1. Phase-Locked Loop: (a) Basic block diagram, (b) Phase noise of a first-order loop with a low noise input

One of the most challenging parts of especially high-frequency PLLs used in wireless communication systems is the prescaler due to the demanding specification of low power consumption and low phase noise at GHz frequencies. Block diagram of a basic PLL is shown in Fig.1(a), where the fixed mode prescaler is embedded into the divider in the feedback loop for the sake of simplicity. The phase noise of a first-order PLL with a low noise input is depicted in Fig.1(b) for the sake of illustrating the effect of the divider phase noise on the output noise of the overall PLL system, [5]. As it is shown in the figure, the phase noise at the output of the divider is multiplied by the square of the divide ratio N when translated to the PLL output phase

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noise. Note that, even though the divider phase noise at offset frequencies larger than the loop bandwidth is suppressed by the loop, the divider phase noise at offsets lower than the loop bandwidth, denoted as ω_{loop}, contributes to the overall phase noise of the PLL. In the state-of-the-art fractional-N frequency synthesizers, the loop bandwidth values are usually at a few tens of kHz and most of the wireless standards have demanding phase noise specifications at offsets lower than a few tens of kHz (e.g., DCS 1800 specification of -80dBc/Hz at 1kHz). This clearly illustrates the need for optimizing the prescalers for low noise.

3. DUAL-MODULUS BiCMOS PRESCALER DESIGN

The block diagram of the dual-modulus prescaler depicted for single-ended processing for the sake of clarity is shown in Fig.2. The input buffer functions as a single-ended to differential converter driving the synchronous divide by 4/5 counter. The output of the synchronous counter drives the divide by 8 extender which is comprised of three consecutive asynchronous divide by 2 stages. The additional logic in the feedback loop between the outputs of the asynchronous dividers and the synchronous divide by 4/5 counter is designed to modify the divide ratio in accordance with the *Mode* signal. Differential ECL-based D flip-flop (DFF) and NOR gates are adopted to improve the immunity to common-mode noise sources such as the noise on the substrate and on the power supply lines.

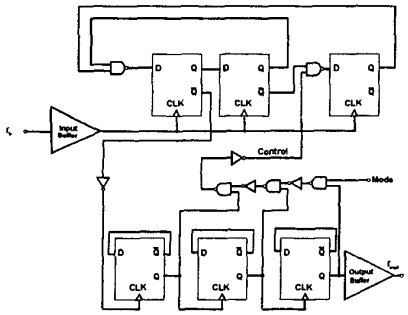

Fig. 2. Block Diagram of the Dual-Modulus Prescaler

The use of ECL level signals in the digital building blocks prove advantageous over the use of CMOS levels in the integrated circuits which accommodate sensitive analog circuits on the same die from the point of view of reducing the disturbance to the sensitive analog signal lines. In the context of the PLL-based frequency synthesizer design, an example of such a sensitive analog signal line is the frequency control input line of the VCO. The switching noise coupled from the prescaler would disturb the VCO output significantly, creating spurs at the synthesizer output. The ECL-level signals would create less noisy disturbances on the substrate than the CMOS-level signals, providing more immunity to the VCO frequency control input.

The biasing of the prescaler is supplied by a bandgap bias generator from which all the bias currents of the building blocks are distributed. The phase noise contribution of the bias generator can be significant, requiring proper measures to be taken to design the circuit for low noise, as it will be clear in the following. The prescaler was designed to process a single-ended signal coming from an off-chip VCO. The input buffer acts like a single-ended to differential converter for this purpose. The output of the input buffer provides the ECL level differential clock signals to the synchronous divide by 4/5 stage. The buffer is a simple differential pair followed by emitter followers to drive the resistive-capacitive loads in the synchronous divide-by-4/5 stage. Note that the buffer should be designed carefully to assure a reasonable input sensitivity with as low of a power consumption as possible.

The DFFs and the NOR gates used in the dividers are all ECL-based building blocks. The schematic of the master-slave DFF is shown in Fig.3. Scaling of the bias currents were done in the dividers in accordance with the frequency of the signals they have to process. The emitter followers were omitted wherever possible to reduce the power consumption. All the gates use minimum emitter size transistors on their signal path to reduce the capacitive loading and thus to minimize the power consumption. To comply with the next generation portable devices, the power supply voltage was tried to be minimized. NMOS transistors were preferred over the bipolar transistors as the tail bias transistors of the gates to reduce the required voltage headroom for minimizing the supply voltage. The circuit that limits the reduction at the power supply voltage is the bandgap generator and 2.5V is used as the supply voltage. The NOR gate which has the off-chip CMOS level Mode signal at one of its inputs is a true BiCMOS gate that works with CMOS levels at one input and ECL levels at the other input.

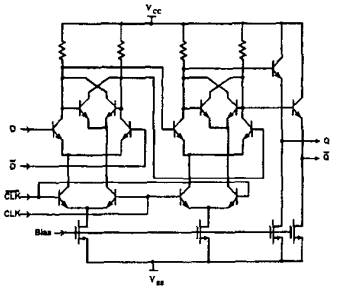

Fig. 3. The ECL-based master and slave DFF

Most important design trade-off in the prescalers is the one between the speed of operation and the power consump-

tion. Special care has been taken in the design to reduce the power consumption of the blocks while guaranteeing proper operation at 2.3GHz. The simulated power consumption contributions of the different sections of the dual modulus prescaler are tabulated in Table 1. The main contributors are the building blocks which run at the maximum input frequency, i.e., the synchronous divide by 4/5 counter and the input buffer. The floorplan of the layout was carefully designed in order to minimize the interconnection capacitances in the critical paths.

Table 1. Simulated power consumption percentage contributions of the Dual-Modulus Prescaler building blocks

Input Buffer	Bias Network	Synchronous Counter	Asynchronous Dividers
24%	8.3%	48.3%	19.2%

The phase noise of the prescaler was investigated through simulations to determine the main noise contributors. The simulated phase noise of the prescaler obtained from Periodic Steady State simulations in SpectreRF of Cadence is shown in Fig.4. As the PLL system the prescaler is aimed to be used in will shape the noise contributed by the prescaler with a lowpass characteristic, the corner frequency of which is determined by the loop bandwidth, the phase noise contribution from the prescaler at low offset frequencies (i.e. the frequencies lower than the loop bandwidth which is usually at a few tens of kHz in the frequency synthesizers used in the wireless communication systems) are of importance.

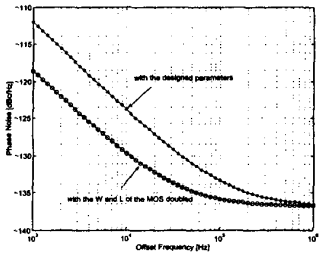

Fig. 4. Simulated Phase Noise of the Prescaler

The main contributors to the phase noise at low offsets are found to be the 1/f noise of the MOS current mirror transistors providing the bias to the divide by 8 extender asynchronous dividers. The diode-connected NMOS tail current mirror transistor biasing the asynchronous dividers contributes around 62% of the total noise at 1kHz and 5kHz offsets. The bias currents of the building blocks are distributed from the bandgap bias generator using PMOS current mirror transistors and the 1/f noise of the PMOS transistors providing the bias to the tail current mirror of the extender asynchronous dividers accounts for about 12% of the total phase noise at both 1kHz and 5kHz offsets. A straightforward way to reduce the 1/f noise of the MOS transistors is to increase the gate lengths and simply by doubling the gate widths and lengths of the MOS transistors, a reduction of about 6dB is obtained in the phase noise at 1kHz and 5kHz offsets as shown in the simulation results given in Fig.4. A better solution to reduce the noise would be to use bipolar transistors at the current mirrors for biasing the ECL gates, as the bipolar devices generate much less 1/f noise than the MOS devices, but this would conflict with the reduction of the supply voltage and hence the power consumption as mentioned earlier. The trade-off between phase noise and power consumption is obvious here.

Note that in Fig.4, no phase noise improvement is observed at the noise floor reached at higher offsets by doubling the gate areas, because an improvement at the noise floor requires a reduction at the thermal noise contributions of the devices by increasing the current consumption, imposing a trade-off between power consumption and the noise floor, [3], [4]. As the PLL suppresses the phase noise of the prescaler at high offset frequencies anyway, it is not advisable to burn more power to reduce the noise floor of the prescaler itself.

4. EXPERIMENTAL RESULTS

The dual-modulus prescaler was designed and fabricated with a 0.6μm BiCMOS process of Texas Instruments. The technology provides NPN transistors with a peak f_T of 22 GHz. The die micrograph of the prescaler is shown in Fig.5. The prescaler including the bias network and the output buffer occupies around 375μm X 350μm of Silicon area excluding the bonding pads.

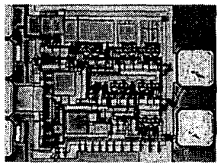

Fig. 5. Die micrograph of the Prescaler

The measurements were taken from parts packaged in Thin Quad Flat Packages (TQFP) with 44 pins. The circuit draws 2.35mA from a 2.5V supply. Out of the 15 packaged parts measured, 13 of them were found functional, giving a yield more than 85%. The maximum operating frequency and the power consumption of the functional parts are roughly within $\pm 5\%$ of the mean values. The differential outputs of the prescaler were taken out of the chip through an emitter-coupled pair buffer with on-chip resistor loads. The buffer is self-biased with an on-chip bias resistor

and it draws around 1.6mA from a separate power supply of 2.5V. The differential outputs are converted into a single-ended signal with a surface mount Balun on the test PCB for the measurement equipment.

The input sensitivity measurements of the prescaler in divide by 33 mode were done with V_{cc}=2.5V at room temperature. The proper division of the circuit was observed from a spectrum analyzer. The measurements show a wide-band frequency range from 100 MHz to 2.4GHz as shown in Fig.6. The increase at the sensitivity at around 1.8GHz is due to the self-oscillation phenomena in the absence of an input signal, as commonly seen in the ECL-based dividers, [3]. The solid lines indicate the maximum and the minimum signal levels required for proper operation at the respective input frequencies. To determine the minimum supply voltage for the prescaler, the input sensitivity versus the supply voltage characteristic was also measured. As plotted in Fig.7, the circuit still operates with a supply voltage of 2.1V, but with quite a limited input sensitivity.

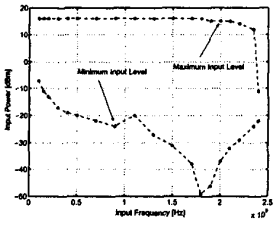

Fig. 6. Measured input sensitivity over the frequency

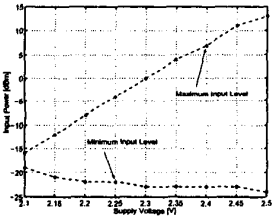

Fig. 7. Measured input sensitivity over the supply voltage

The phase noise of the prescaler was measured with an RDL NTS-1000B phase noise measurement system. Phase noise values of -107.6dBc/Hz and -120.1dBc/Hz were measured at 1kHz and 5kHz offsets, respectively, as shown in Fig.8. The values correspond to contributions of around -77dBc/Hz and -89.7dBc/Hz at 1kHz and 5kHz offsets to the phase noise of a PLL using this prescaler. The noise at 1kHz offset is short of meeting the DCS specifications. The circuit requires noise optimization to be done using the guidelines provided briefly in the previous section. In the same figure, the simulated phase noise is also plotted. The match between the simulated and the measured results are within 5dB for offsets ranging from 1kHz to 1MHz. Note that good consistency is observed between the simulated and measured data within the 1/f noise region where the noise due to the prescaler is not suppressed by the PLL.

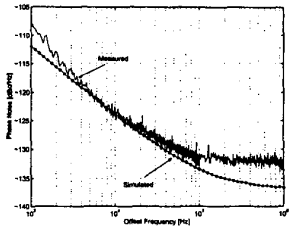

Fig. 8. Measured vs. simulated phase noise of the Prescaler in divide-by-33 mode with $f_{in} = 2.35$GHz

5. CONCLUSIONS

Design considerations of a dual-modulus divide by 32/33 prescaler in BiCMOS are presented. The phase noise contributors in the circuit determined through simulations are investigated and some guidelines are provided to improve the noise performance. The impact of the integrated bias network on the phase noise of the prescaler is demonstrated together with the trade-off between the power consumption and the phase noise.

6. REFERENCES

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